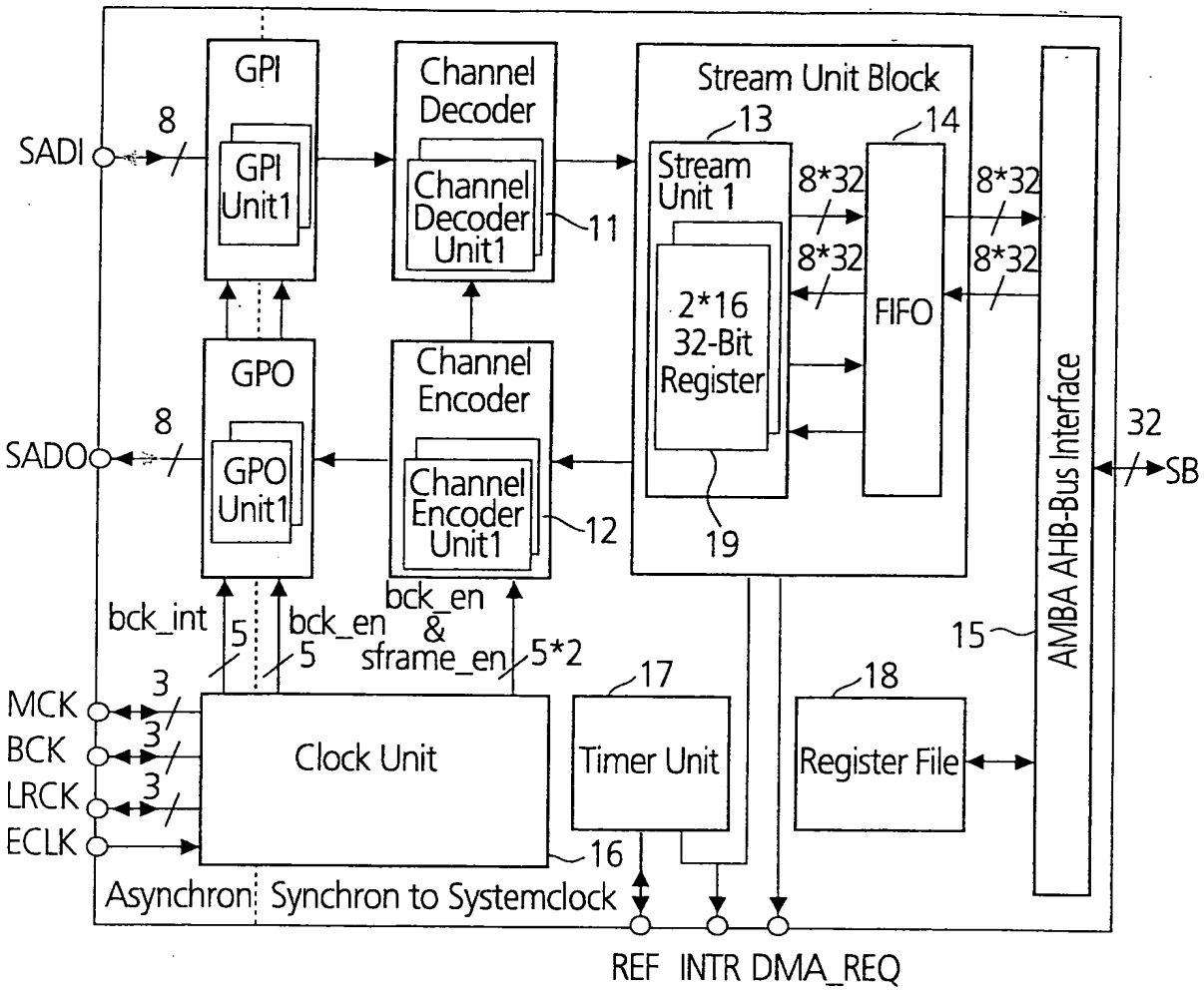

GPI
Channel Decoder
Stream Unit Block
SADI
8
GPI Unit1
Channel Decoder Unit1
11
13
14
Stream Unit 1
8*32
8*32
8*32
8*32
2*16 32-Bit Register
FIFO
GPO
Channel Encoder
8
SADO
GPO Unit1
Channel Encoder Unit1
12
19
32
SB
AMBA AHB-Bus Interface
bck_int
5
bck_en
5
bck_en & sframe_en
5*2
15
3
MCK
3
BCK
3
LRCK
ECLK
Clock Unit
17
Timer Unit
18
Register File
16
Asynchron
Synchron to Systemclock
REF
INTR
DMA_REQ

Fig.1

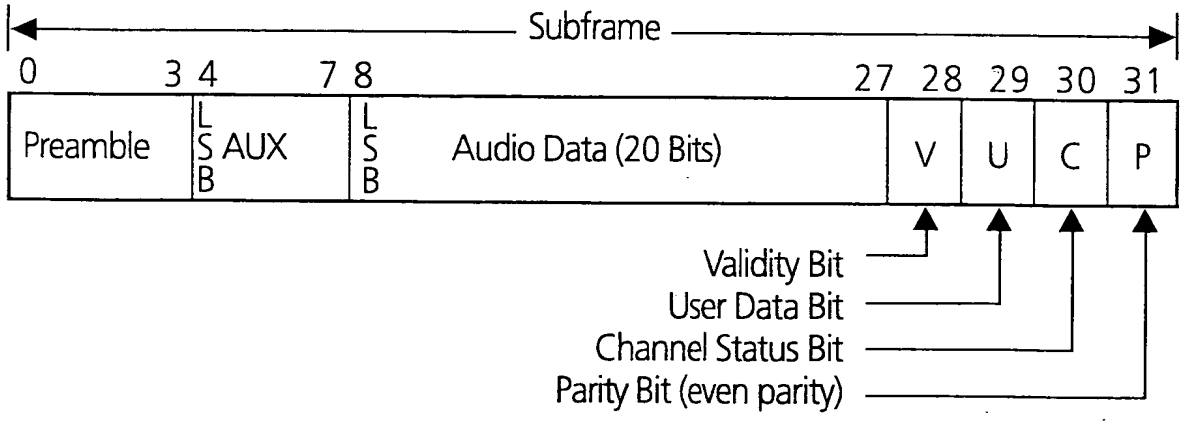

Subframe
0
3 4
7 8
27 28 29 30 31
Preamble
LSB AUX
LSB
Audio Data (20 Bits)
V
U
C
P
Validity Bit
User Data Bit
Channel Status Bit
Parity Bit (even parity)

Fig.2

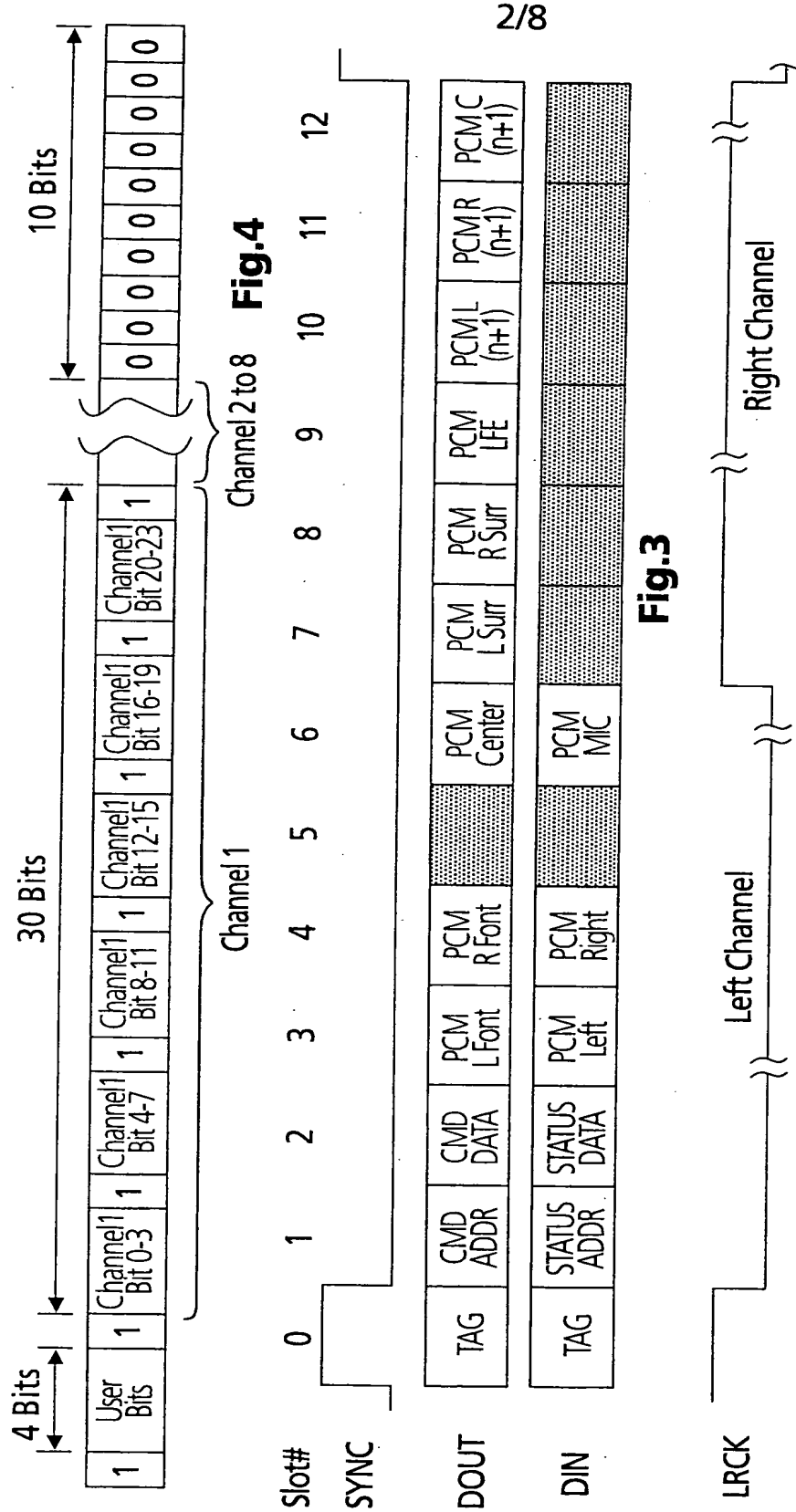


Fig.4

Fig.3

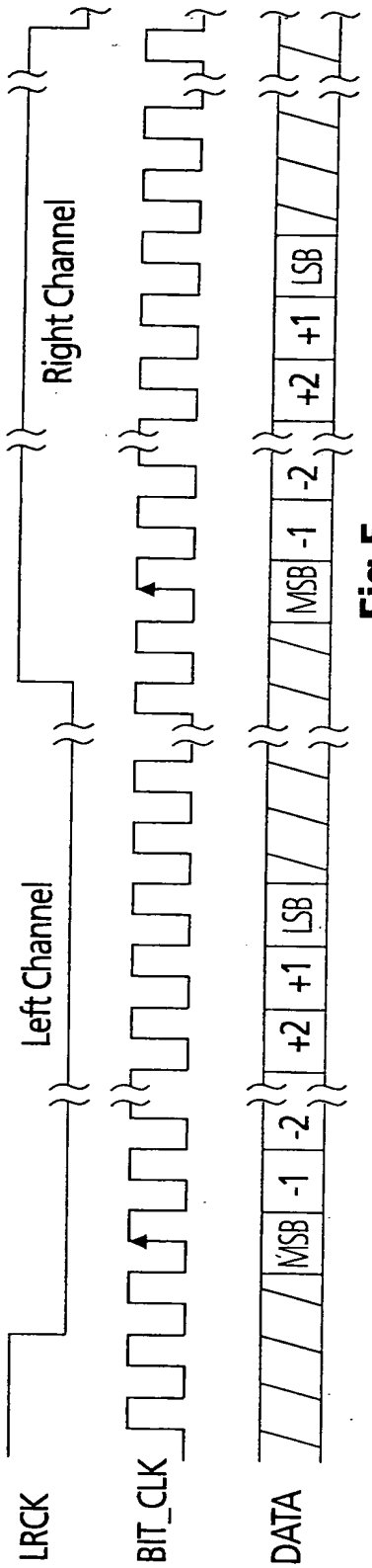


Fig.5

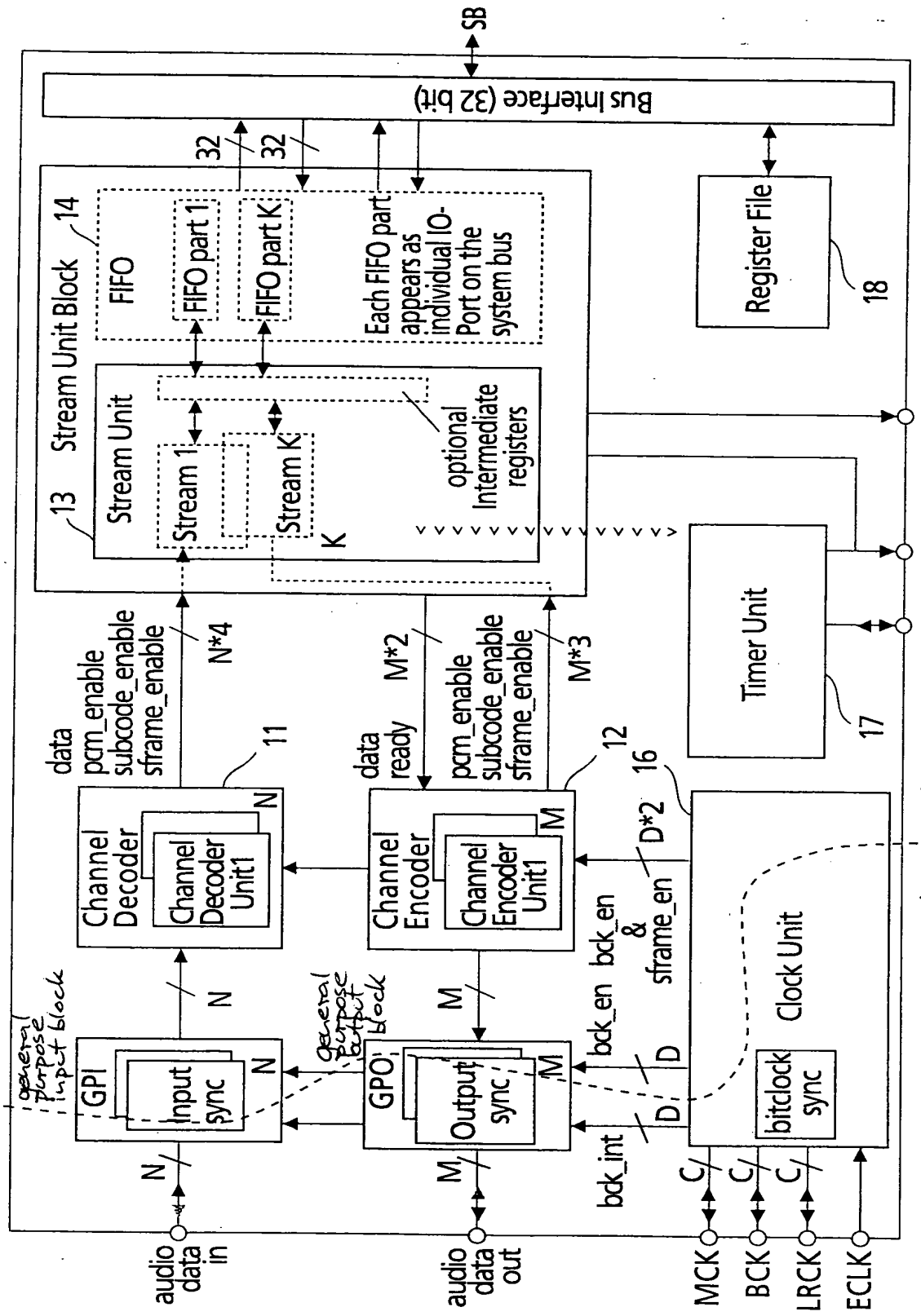

SB
Bus Interface (32 bit)
32
32
Stream Unit Block
14
FIFO
FIFO part 1
FIFO part K
Each FIFO part appears as individual IO-Port on the system bus
13
Stream Unit
Stream 1
Stream K
K
optional Intermediate registers
Register File
18
data
pcm_enable
subcode_enable
sframe_enable
N*4
M*2
data ready
pcm_enable
subcode_enable
sframe_enable
M*3
Timer Unit
17
11
12
16
Channel Decoder
Channel Decoder Unit1
N
Channel Encoder
Channel Encoder Unit1
M
D*2
bck_en
&
sframe_en
asynchron synchronized to system clock
REF
INTR
DMA_REQ
general purpose input block
GPI
Input sync
N
general purpose output block
GPO
Output sync
M
bck_en
D
bck_int
D
Clock Unit
bitclock sync
C
C
C
audio data in
audio data out
MCK
BCK
LRCK
ECLK

Fig.6

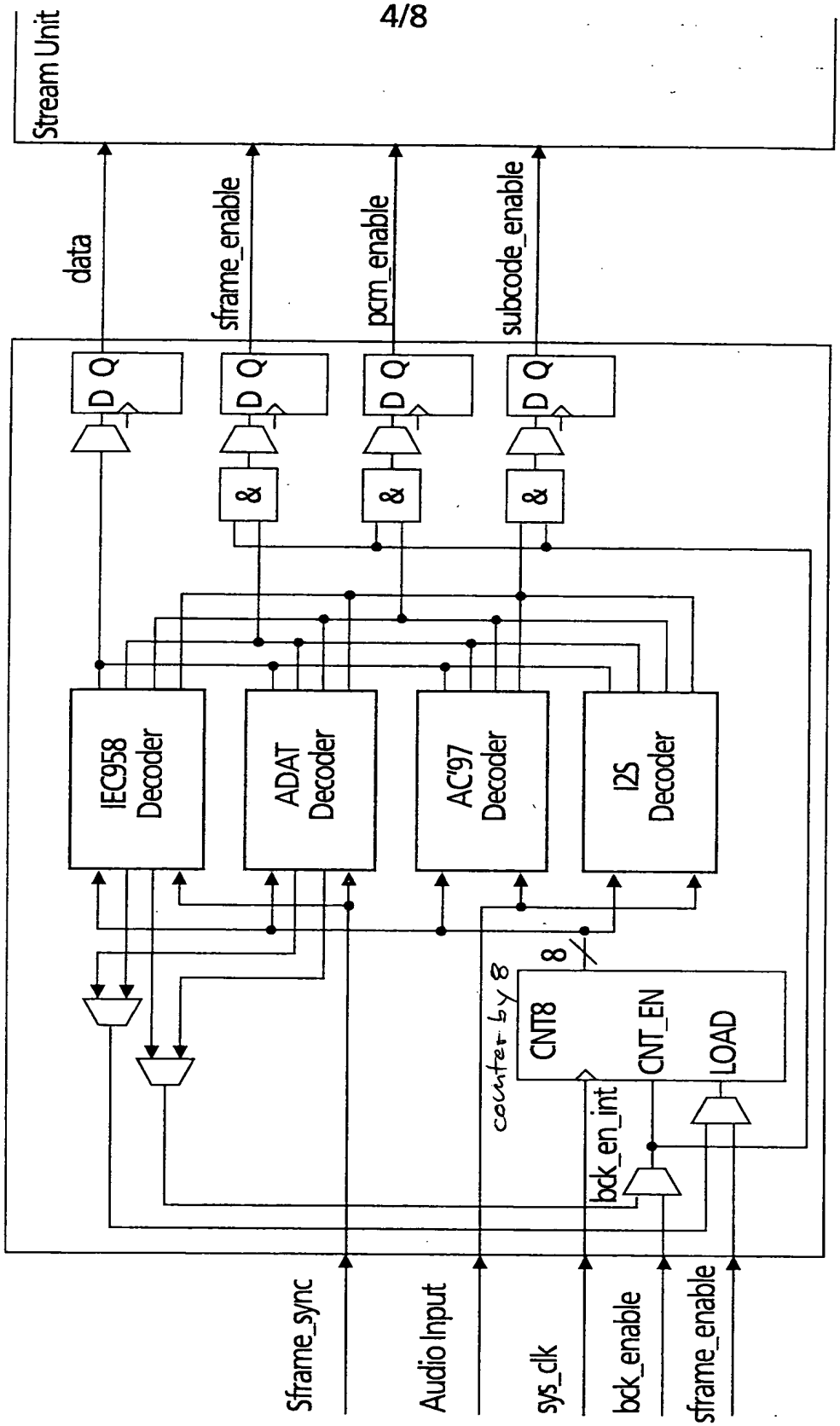

Stream Unit
data
sframe_enable
pcm_enable
subcode_enable
D Q
&
IEC958 Decoder
ADAT Decoder
AC'97 Decoder
I2S Decoder
8
counter by 8
CNT8
CNT_EN
LOAD
bck_en_int
Sframe_sync
Audio Input
sys_clk
bck_enable
sframe_enable

Fig.7

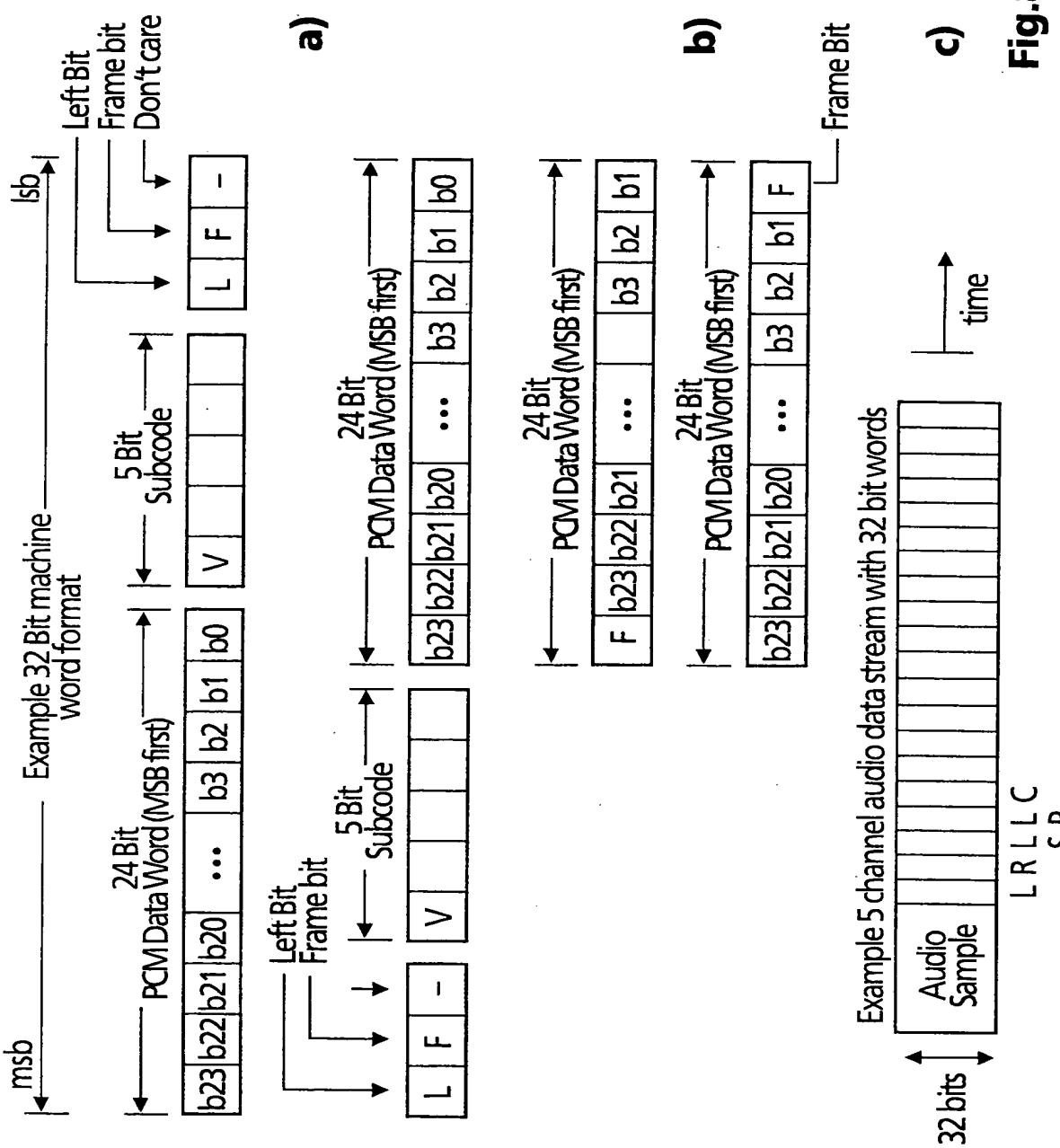

msb
lsb
Example 32 Bit machine word format
Left Bit
Frame bit
Don't care
24 Bit PCM Data Word (MSB first)
5 Bit Subcode
b23 b22 b21 b20 ... b3 b2 b1 b0
V
L F -
a)
Left Bit
Frame bit
5 Bit Subcode
24 Bit PCM Data Word (MSB first)
L F -
V
b23 b22 b21 b20 ... b3 b2 b1 b0
24 Bit PCM Data Word (MSB first)
F b23 b22 b21 ... b3 b2 b1
b)
24 Bit PCM Data Word (MSB first)
b23 b22 b21 b20 ... b3 b2 b1 F
Frame Bit
Example 5 channel audio data stream with 32 bit words
32 bits
Audio Sample
L R L L C
S R
time
c)

Fig.8

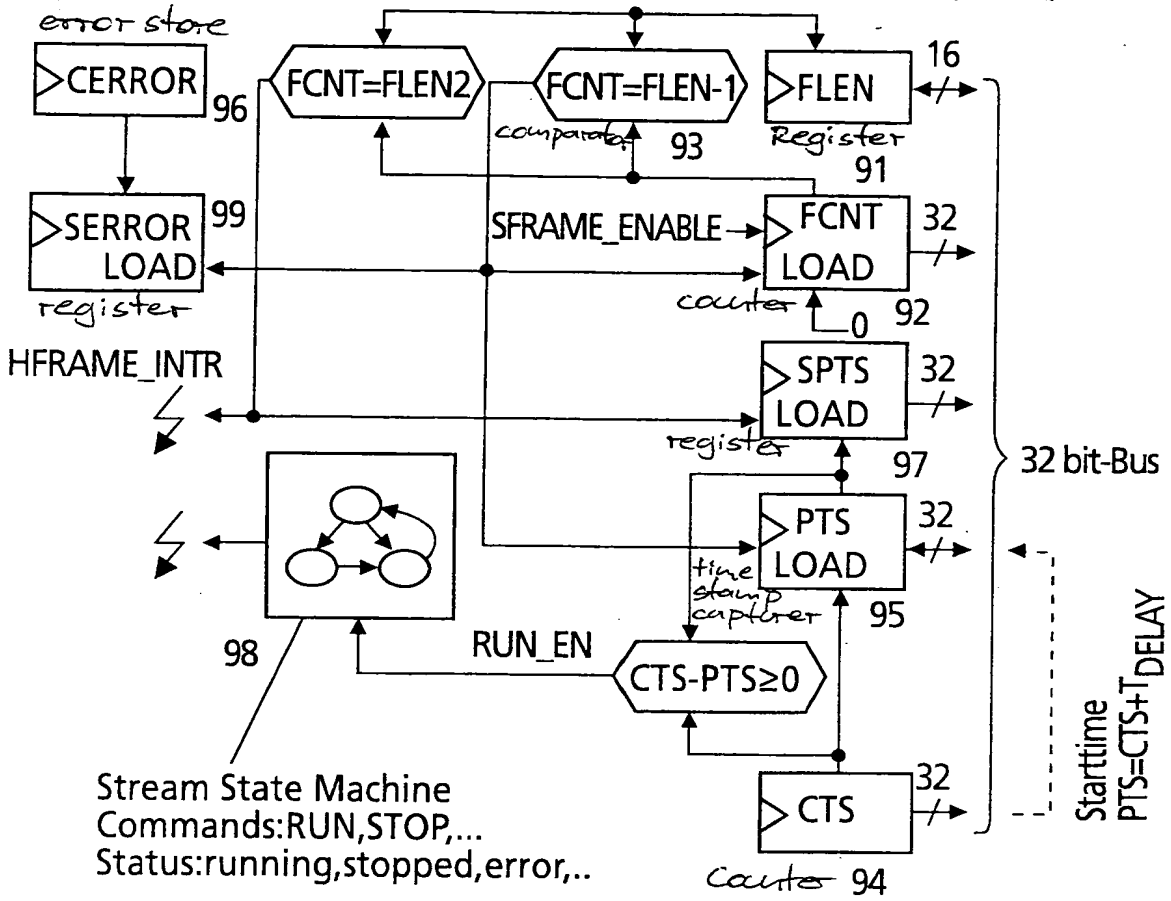

error store
CERROR
96
FCNT=FLEN2
FCNT=FLEN-1
comparator
93
FLEN
Register
16
91
SERROR LOAD
99
register
SFRAME_ENABLE
FCNT LOAD
32
counter
0
92
HFRAME_INTR
SPTS LOAD
32
register
97
32 bit-Bus
PTS LOAD
32
time stamp capturer
95
98
RUN_EN
CTS-PTS≥0
Stream State Machine
Commands:RUN,STOP,...
Status:running,stopped,error,..
CTS
32
Counter
94
Starttime
PTS=CTS+T_DELAY

Fig.9

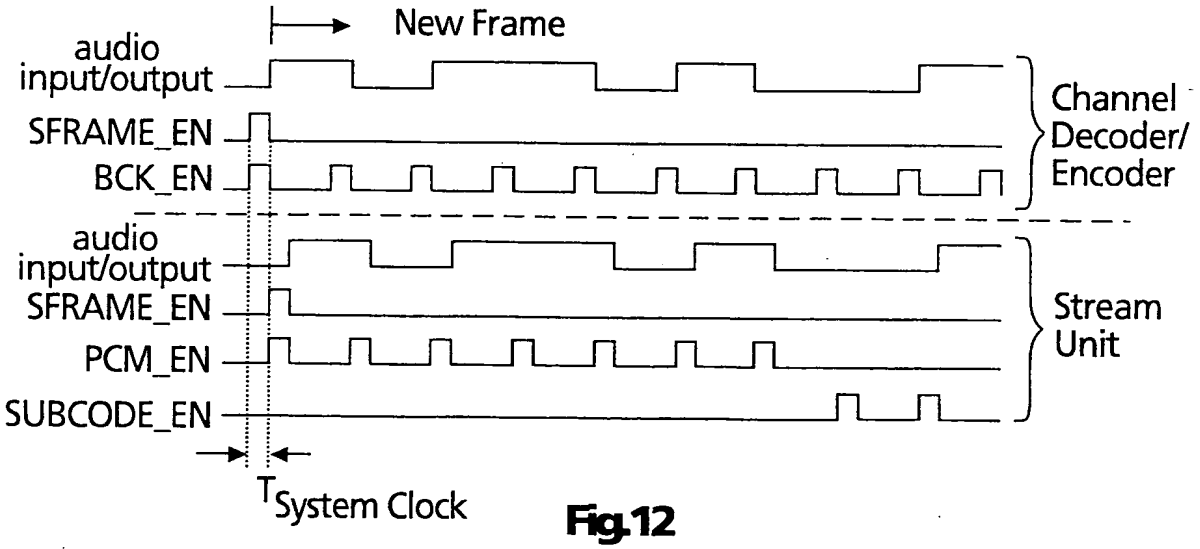

New Frame
audio input/output
SFRAME_EN
BCK_EN
Channel Decoder/ Encoder
audio input/output
SFRAME_EN
PCM_EN
SUBCODE_EN
Stream Unit
T System Clock

Fig.12

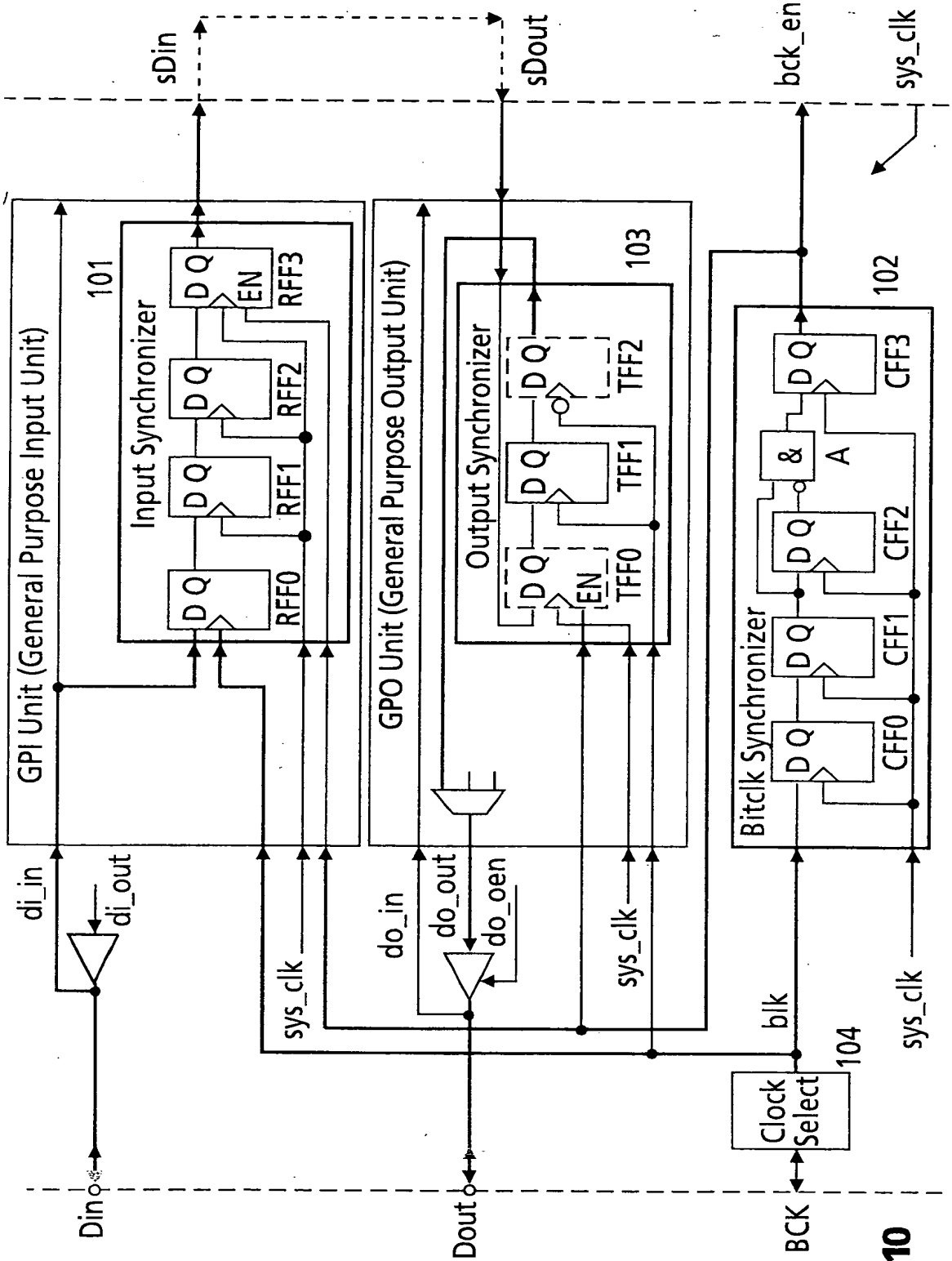
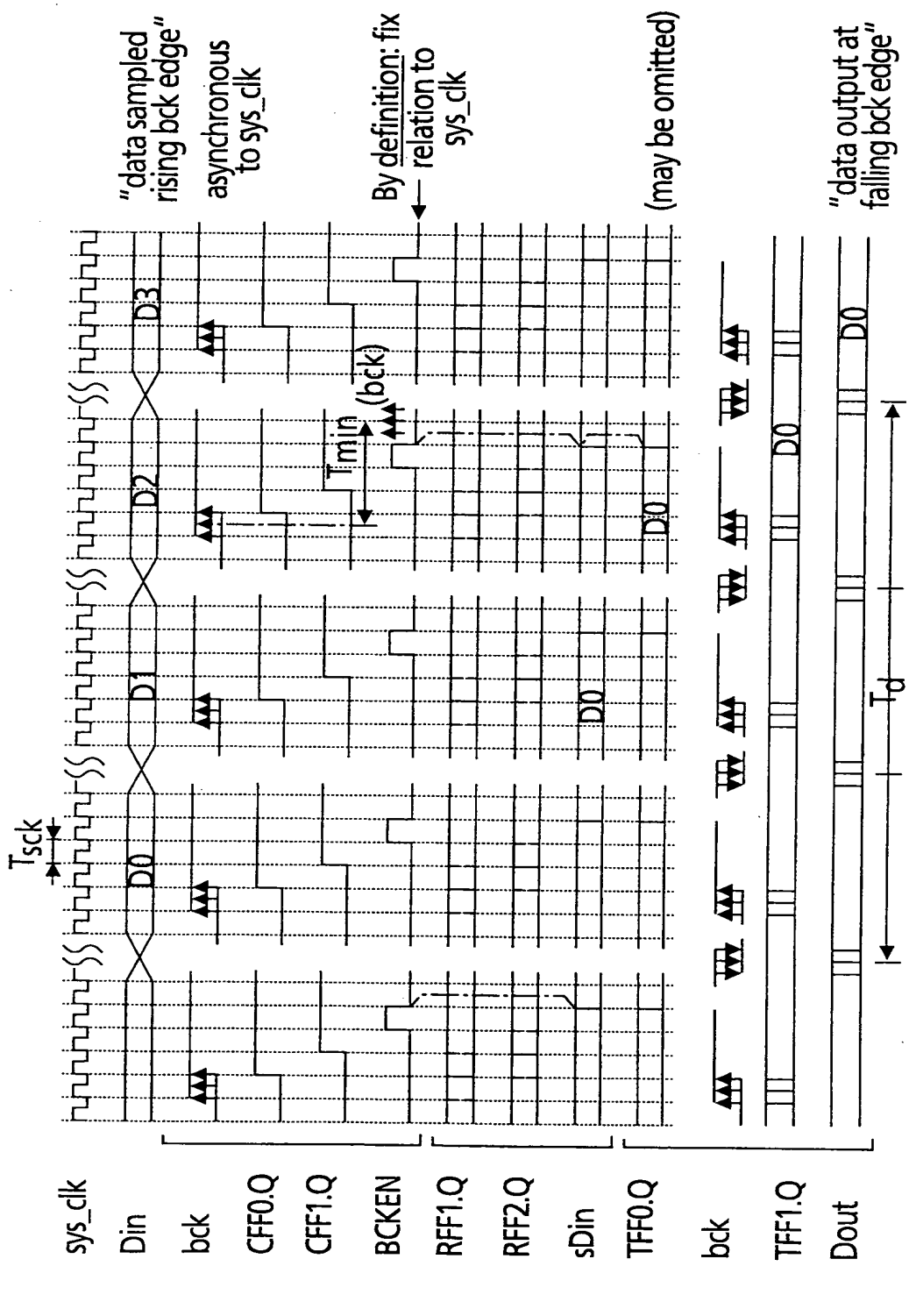

sDin
sDout
bck_en
sys_clk
GPI Unit (General Purpose Input Unit)
101
Input Synchronizer
D Q
EN
RFF3
RFF2
RFF1
RFF0
GPO Unit (General Purpose Output Unit)
103
Output Synchronizer
TFF2
TFF1
TFF0
102
Bitclk Synchronizer
&
A
CFF3
CFF2
CFF1
CFF0
di_in
di_out
do_in
do_out
do_oen
sys_clk
blk
104
Clock Select
Din
Dout
BCK

Fig.10



Constant Synchronizer Data delay: using opt. TFF0 : 3 bck cycles --if-- $T_{min} > 4*T_{sck} + (T_{clkToOut} + T_{setup} + T_{safety})$ (i.e. $F_{sysclk} > (4.x)*F_{bck}$)
without/bypassing: 2 bck cycles
T_d

Fig.11